UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,288	09/06/2000	Oscar R. Herrera E.	10001963-1	9450

22879 7590 04/25/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
MOE, AUNG SOE	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/656,288	HERRERA E., OSCAR R.	
	Examiner	Art Unit	
	Aung S. Moe	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Please note that this application has been assigned to a different Examiner.

Response to Arguments

1. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, and 6-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamasaki (U.S. Pat. No. 5,335,008).

Regarding claim 1, Hamasaki '008 discloses a system (Fig. 1) for optically imaging, the system comprising:

an array of cells (i.e., noted the pixel elements 5 arranged in a two-dimensional fashion; see col. 2, lines 60+) for producing an electrical charge in response to photo stimulation (i.e., noted the CCD sensing device as discussed in col. 1, lines 25+ and col. 2, lines 60+ is capable of producing an electrical charges as claimed);

a charge shift register configured to receive the electrical charge produced by each cell (i.e., the pixel 5 of Fig. 1) in the array and to sequentially output the electrical charge of each cell (as shown in Fig. 1, with the use of the elements RG, the vertical register 9 are capable of sequentially shifting the charge of each pixel cell to the output 10; see col. 3, lines 20-30);

at least two charge sensing nodes (i.e., noted the each charge sensing node of capacitors C1 and C2) for accumulating charge readable, from each charge sensing node, as a voltage (i.e., noted that the capacitors C1 & C2 are holding the charge, e.g., Vout, so that the charge can be read as voltage; see col. 3, lines 20-30 and col. 4, lines 1-15); and

a charge demultiplexor (i.e., noted the switch 14 of Fig. 1) configured to receive the output charge (i.e., Vout as shown in Fig. 1) of the charge shift register (9) and to selectively distribute the output charge to each of the at least two charge sensing node (i.e., noted that the switch 14 is functioned as a charge demultiplexor to selectively distributing the output charges to the capacitor nodes C1 and C2; see Fig. 1 and col. 4, lines 1-15).

Regarding claim 2, Hamasaki '008 discloses wherein the array of cells includes a charge coupled device array (i.e., Fig. 1; col. 1, lines 24+ and col. 2, lines 60+).

Regarding claim 3, Hamasaki '008 discloses at least one output buffer configured to receive the voltage of each of at least two charge-sensing nodes (i.e., noted that the buffer amplifier 16 as shown in Fig. 1 is used to receive the voltage output, e.g., Vout, of each of at least two nodes C1 & C2).

Regarding claim 4, Hamasaki '008 discloses at least one amplifier configured to amplify the voltage from the at least two charge sensing node ((i.e., noted that the buffer amplifier 16 as shown in Fig. 1 is used to receive the Vout of each of at least two nodes C1 & C2).

Regarding claim 6, Hamasaki '008 discloses a method for producing a voltage signal (i.e., note Vout as shown in Fig. 1) segment to represent an output of an array of cells (i.e., noted the matrix configuration of pixel array as discussed in col. 2, lines 60+) that produce a cell electrical charge in response to photo stimulation (i.e., noted the CCD sensing device as discussed in col. 1, lines 25+ and col. 2, lines 60+ is capable of producing an electrical charges as claimed), the method comprising:

receiving each of the cell electrical charges from the cells in a charge shift register (i.e., noted the electrical charges received in the vertical shift register 9 as shown in Fig. 1; see col. 3, lines 10-30);

sequentially outputting the cell electrical charges from the charge shift register (Fig. 1, the elements RG and the vertical register 9 are capable of sequentially shifting the charge of each pixel cell to the output 10; see col. 3, lines 20-30) to a charge demultiplexor (i.e., noted that the switch 14 is capable of receiving the charges, e.g., Vout, from the shift register 9);

the charge demultiplexor (14) selectively distributing the sequentially cell charges to one of at least two charge sensing nodes (i.e., noted that the switch 14 is functioned as a charge demultiplexor to selectively distributing the output charges to the capacitor nodes C1 and C2; see Fig. 1 and col. 4, lines 1-15); and

sequentially reading a voltage produced by the cell charges in at least one of the at least two charge sensing nodes (i.e., as discussed above, the shift register 9 is capable of sequentially reading out a voltage, e.g., Vout, produced by the cell charges in one of the two charge sensing capacitor nodes C1 and C2, selectively by the demultiplexor switch 14 as shown in Fig. 1; see col. 3, lines 20-30 and col. 4, lines 1-20).

Regarding claim 7, Hamasaki '008 discloses wherein the charge demultiplexor selectively distributing the sequential cell charges (col. 3, lines 20-30) to one of at least two charge sensing nodes (i.e., the C1 and C2) includes the charge demultiplexor distributing one cell charge (i.e., the charge read out from the cell 5 as shown in Fig. 1) to each of the at least two charge sensing nodes (i.e., see col. 4, lines 4-15).

Regarding claim 8, Hamasaki '008 discloses wherein the charge demultiplexor selectively distributing the sequential cell charges (col. 3, lines 20-30) to one of at least two charge sensing nodes (i.e., the nodes C1 and C2) includes the charge demultiplexor distributing multiple cell charges to each of the at least two charge sensing nodes (i.e., see col. 4, lines 1-15).

Regarding claim 9, Hamasaki '008 discloses a system for producing a voltage signal segmented to represent an output of an array of cells (i.e., noted the Vout signal outputted form the pixel arrays as shown in Fig. 1) that produce an electrical charge in response to photon stimulation (i.e., noted the CCD sensing device as discussed in col. 1, lines 25+ and col. 2, lines 60+ is capable of producing an electrical charges as claimed), the system comprising:

a charge shift register (i.e., noted the vertical shift register 9 as shown in Fig. 1) configured to sequentially receive the charge form the cell (as shown in Fig. 1, with the use of the elements RG, the vertical register 9 are capable of sequentially shifting the charge of each pixel cell to the output 10; see col. 3, lines 20-30);

at least two charge sensing nodes configured to accumulate charge (i.e., noted the each charge sensing node of capacitors C1 and C2 as shown in Fig. 1; see col. 3, lines 20-30 and col. 4, lines 1-15) and output a voltage signal (i.e., noted the output voltage from the CCD sensor,

e.g., Vout, as shown in Fig. 1 is further accumulated in the node capacitors C1 and C2, thus, the voltage signal can be outputted form the node capacitors C1 and C2);

a charge demultiplexor (i.e., noted the switch 14) configured to sequentially distribute each charge from the charge shift register (9) to one of the at least two charge sensing nodes (i.e., noted that the switch 14 is functioned as a charge demultiplexor to selectively distributing the output charges to the capacitor nodes C1 and C2; see Fig. 1 and col. 4, lines 1-15).

Regarding claim 10, Hamasaki '008 discloses at least one output buffer configured to receive the voltage of each of the at least two charge sensing node (i.e., noted that the **buffer** amplifier 16 as shown in Fig. 1 is used to receive the voltage output, e.g., Vout, of each of at least two nodes C1 & C2).

Regarding claim 11, Hamasaki '008 discloses at least one amplifier configured to receive and amplify the voltage of each of the at least two charge sensing nodes (i.e., noted that the buffer **amplifier 16** as shown in Fig. 1 is used to receive the voltage output, e.g., Vout, of each of at least two nodes C1 & C2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 12, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki '008 in view of Sawanobori (U.S. 5,956,086).

Regarding claim 5, it is noted that Hamasaki '008 does not explicitly stated the use of an A/D converter for converting the voltage into a digital signal.

However, the above-mentioned clamed limitations are well known in the art as evidenced by Sawanobori '086. In particular, Sawanobori '086 teaches the use of an A/D converter (i.e., see Fig. 1, the element 18; see col. 4, lines 65+) for converting the voltage from at least two charge sensing nodes (i.e., noted the node capacitors 45 and 46 as shown in Fig. 4; col. 8, lines 5-15) so that an analog signal can be converted to binary code and provide further advantages such that improved resolution/quality of image, high-speed readout and reduce manufacturing cost (i.e., col. 1, lines 40-45).

In view of the above, having the system of Hamasaki '008 and then given the well-established teaching of Sawanobori '086, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Hamasaki '008 as taught by Sawanobori '086, since it is clearly obvious to one skilled in the art that such a modification would improve resolution/quality of image and reduce manufacturing cost (i.e., see col. 1, lines 40+ of Sawanobori '086).

Regarding claim 12, please see the Examiner's comments with respect to claim 5 as discussed above.

Regarding claim 13, it is noted that although Hamasaki '008 discloses that at lest one of the charges sensing nodes (i.e., the capacitors C1 and C2) is configured to held the output charge of the even/odd lines respectively (i.e., col. 4, lines 1-15), Hamasaki '008 does not explicitly

stated that *the electrical charge are summed at one of the charge sensing node* as recited in the present claimed invention.

However, the above-mentioned clamed limitations are well known in the art as evidenced by Sawanobori '086. In particular, Sawanobori '086 teaches the use of at least two charge sensing nodes (i.e., noted the nodes 45 and 46 of Fig. 6; see col. 8, lines 1-15) for summing the electrical charge output from the CCD sensor (12) respectively (i.e., see col. 8, lines 5+ and col. 9, lines 50+; see Figs. 5 and 6 of Sawanobori '086).

In view of the above, having the system of Hamasaki '008 and then given the well-established teaching of Sawanobori '086, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Hamasaki '008 as taught by Sawanobori '086, since Sawanobori '086 stated in col. 1, lines 40+ that such a modification would reduce manufacturing cost thereof (i.e., see col. 1, lines 40+ of Sawanobori '086).

Regarding claim 14, it is noted that although Hamasaki '008 discloses that at lest one of the charges sensing nodes (i.e., the capacitors C1 and C2) is configured to held the output charge of the even/odd lines before they are sequentially read out (i.e., col. 4, lines 1-15), Hamasaki '008 does not explicitly stated that "summing at least two of the distributed cell charges on at least one of the charge sensing node" as recited in present claimed invention.

However, the above-mentioned clamed limitations are well known in the art as evidenced by Sawanobori '086. In particular, Sawanobori '086 teaches the summing of at lest two of the distributed cell charges (i.e., noted the summed output signals as shown in Figs. 5 and 6) on at least one of the charge sensing nodes (i.e., noted the nodes 45 and 46 of Fig. 6; see col. 8, lines

1-15) before sequentially reading the voltage produced by the cell charges (i.e., noted the sequentially reading of the charge voltage produced the sensor cell 12; see col. 8, lines 5+ and col. 9, lines 50+ and Figs. 4, 5 and 6 of Sawanobori '086).

In view of the above, having the system of Hamasaki '008 and then given the well-established teaching of Sawanobori '086, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Hamasaki '008 as taught by Sawanobori '086, since Sawanobori '086 stated in col. 1, lines 40+ that such a modification would reduce manufacturing cost thereof (i.e., see col. 1, lines 40+ of Sawanobori '086).

Regarding claim 15, please see the Examiner's comments with respect to claims 13 and 14 as discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Mon-Fri (9-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2612

A. Moe
April 19, 2005